CLAIMS

What is claimed is:

1. A method comprising:

issuing one or more command(s) to one or more inputs of a general purpose input/output (GPIO) system, wherein the command(s) cause a first output of the GPIO system associated with a first input of the inputs to issue a control signal to a latch associated with a port bypass circuit (PBC), and a second output of the GPIO system associated with a second of the inputs of the GPIO system to issue a clock signal to a latch associated with a PBC addressed by the received command(s); and

setting the state of the PBC with the received control signal if the control signal and the clock signal are consistent to change the state of the PBC.

2. A method according to claim 1, wherein the control signal changes a state of the PBC.

3. A method according to claim 1, wherein the command is sent to a first GPIO device within the GPIO system to generate the first output, and to a second GPIO device within the GPIO system to issue the second output.

4. A method according to claim 1, wherein the state of the PBC does not change unless the command is accurately received and a single latch associated with the PBC is addressed.

5. A method according to claim 1, wherein the command is a serial bus command addressing the PBC.

6. A method according to claim 1, wherein the command is an I^2C command addressing the PBC.

7. A storage device comprising a plurality of executable instructions at least a subset of which, when executed, implement a method including:

issuing one or more command(s) to one or more inputs of a general purpose input/output (GPIO) system, wherein the command(s) cause a first output of the GPIO system associated with a first input of the inputs to issue a control signal to a latch associated with a port bypass circuit (PBC), and a second output of the GPIO system associated with a second of the inputs of the GPIO system to issue a clock signal to a latch associated with a PBC addressed by the received command(s); and

setting the state of the PBC with the received control signal if the control signal and the clock signal are consistent to change the state of the PBC.

8. A storage system comprising:

a memory device having stored therein a plurality of executable instructions; and

an execution unit, coupled to the memory device, to execute at least a subset of the plurality of executable instructions to issue one or more command(s) to one or more inputs of a general purpose input/output (GPIO) system, wherein the command(s) cause a first output of the GPIO system associated with a first input of the inputs to issue a control signal to a latch associated with a port bypass circuit (PBC), and a second output of the GPIO system associated with a second of the inputs of the GPIO system to issue a clock signal to a latch associated with a PBC addressed by the received command(s), and set the state of the PBC with the received control signal if the control signal and the clock signal are consistent to change the state of the PBC.

9. A method comprising:

issuing one or more control command(s) to a controller which, when interpreted causes the controller to issue control signals to a port bypass circuit to control an operational state of the port bypass circuit; and

verifying that the controller accurately received the one or more control commands before the control signals are passed to the port bypass circuit.

10. A method according to claim 9, wherein issuing one or more control commands comprises:

constructing the one or more control commands in accordance with an error checking protocol.

11. A method according to claim 10, wherein the error checking protocol includes zero or more of calculating a cyclical redundancy check (CRC) value for each command, or encoding each command.

12. A storage device comprising a plurality of machine executable instructions at least a subset of which, when executed, implement a method including:

issuing one or more control command(s) to a controller which, when interpreted causes the controller to issue control signals to a port bypass circuit to control an operational state of the port bypass circuit; and

verifying that the controller accurately received the one or more control commands before the control signals are passed to the port bypass circuit.

13. A storage system comprising:

a controller, to issue a command to change a state of a port bypass circuit (PBC); and

a general purpose input/output (GPIO) system, coupled to the controller, to receive the issued command via a first input and a second input, to generate a control signal to a latch associated with a PBC addressed by the command

received via the first input, and to generate a clock signal to a latch associated with a PBC addressed by the command received via the second input, wherein the state does not change unless the first input and the second input receive the command unchanged.

5

14. A storage system according to claim 13, wherein the GPIO system comprises two GPIO devices, one associated with the first input and another associated with the second input.